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Question Paper Code : 81228

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2025.

Third Semester

Electrical and Computer Engineering

EC 3301 — ELECTRON DEVICES AND CIRCUITS

(Common to : Electrical and Electronics Engineering)

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. What is the difference between a rectifier and a regulator?
2. List the semiconductor materials used in LED.
3. Why is IGBT preferred for high power applications?
4. What is a thyristor and where is it used?
5. What is the need for coupling capacitors in amplifier design?
6. What is Miller's theorem?
7. What is the need for constant current source in a differential amplifier?
8. What should be the value of A_c , the common mode gain and A_d the difference mode gain for an ideal differential amplifier?
9. When is a tuned circuit resistive, capacitive and inductive?
10. A feedback amplifier has a open loop gain of 600 and feedback factor of 0.01. Find the closed loop gain with negative feedback.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Discuss how diode limiters and diode clampers differ in terms of their function. (4)
- (ii) A sinusoidal input voltage $V_{in}(t) = 10 \sin(\omega t)$ is applied to a circuit that consists of a positive clamper and a positive clipper that limits the voltage to no more than +12V. Determine the output waveform after the clamper and after the clipper. Also sketch and describe the final waveform. (9)

Or

- (b) A full-wave bridge rectifier with a 120-V rms sinusoidal input has a load resistor of 1K.
- (i) If silicon diodes are employed, what is the dc voltage available at the load? (3)
- (ii) Determine the required PIV rating of each diode. (3)
- (iii) Find the maximum current through each diode during conduction and what is the required power rating of each diode. (7)
12. (a) Design a voltage-divider bias network using a supply of 24 V, a CE transistor with a beta of 110, an operating point of $I_{CQ} = 4 \text{ mA}$ and $V_{CEQ} = 8 \text{ V}$. Choose $V_E = 1/8 V_{CC}$. Use standard values.

Or

- (b) Given $I_{DSS} = 6 \text{ mA}$ and $V_P = -4.5 \text{ V}$. Sketch the transfer characteristics for :
- (i) Determine I_D at $V_{GS} = -2$ and -3.6 V . (7)
- (ii) Determine V_{GS} at $I_D = 3$ and 5.5 mA . (6)
13. (a) For the CE voltage-divider configuration circuit with values $V_{CC} = 16 \text{ V}$, $C_{C1} = 6.8 \mu\text{F}$, $R_C = 2.2 \text{ K}\Omega$, $R_E = 0.75 \text{ K}\Omega$, $C_E = 10 \mu\text{F}$, $C_{C2} = 6.8 \mu\text{F}$, $R_L = 5.6 \text{ K}\Omega$, $R_{B1} = 68 \text{ K}\Omega$ and $R_{B2} = 16 \text{ K}\Omega$.
- (i) Determine A_{vNL} , Z_i and Z_o and sketch the two-port model. (7)
- (ii) Calculate the gain A_v and determine the current gain A_i . (6)

Or

- (b) Determine the high cutoff frequencies for the CS JFET Amplifier with parameters $C_G = 0.01 \mu\text{F}$, $C_C = 0.5 \mu\text{F}$, $C_S = 2 \mu\text{F}$, $R_{sig} = 10 \text{ k}\Omega$, $R_G = 1 \text{ M}\Omega$, $R_D = 4.7 \text{ k}\Omega$, $R_S = 1 \text{ k}\Omega$, $R_L = 2.2 \text{ k}\Omega$, $I_{DSS} = 8 \text{ mA}$, $V_P = -4 \text{ V}$, $r_d = \infty \Omega$, $V_{DD} = 20 \text{ V}$ with the addition of $C_{gd} = 2 \text{ pF}$, $C_{gs} = 4 \text{ pF}$, $C_{ds} = 0.5 \text{ pF}$, $C_{w1} = 5 \text{ pF}$, $C_{w2} = 6 \text{ pF}$.

14. (a) The differential amplifier has the following values $R_C = 50 K$, $R_e = 100 K$ and $R_s = 10 K$. The transistor parameters are $r_\pi = 50 K = h_{ie}$, $h_{fe} = \beta_o = 2 \times 10^3$, $r_o = 400 K$. Determine A_d , A_c and CMRR in db.

Or

- (b) Design a tuned amplifier using FET to have $f_o = 1 \text{ MHz}$, 3 dB bandwidth of 10 kHz, maximum gain of -10, $g_m = 5 \text{ mA/V}$ and $r_d = 10 K$.
15. (a) A Hartley oscillator is designed with $L_1 = 2 \text{ mH}$, $L_2 = 20 \mu\text{H}$ and a variable capacitance. Find the range of capacitance value if the frequency of oscillation is varied between 950 to 2050 KHZ.

Or

- (b) Draw a CE amplifier circuit exhibiting current series feedback and obtain the expression for feedback ratio, voltage gain, input and output resistances.

PART C — (1 × 15 = 15 marks)

16. (a) Design a simple power supply that provides a regulated voltage using a Zener diode suitable for powering low current devices such as LED.

Or

- (b) Illustrate BJT with positive feedback and BJT with negative feedback using suitable diagrams and with an example.

